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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/976,491	DORSEY, MICHAEL C.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☒ Claim(s) *1 & 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3-27-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-32 are presented for examination.

Information Disclosure Statement

The examiner has considered the applicant's Disclosure Statements of 3/27/2003.

Drawings

1. The drawings are objected to because:

   a. FIG.1 memory components 190 are labeled 190a-d in the disclosure.

   b. FIG.2 LSSD and STEP CLKS are not referred to in the disclosure.

   c. FIG.9 LSSD_CLKA, LSSD_CLKB, LBST_SCAN_CLKA and LBST_SDCAN_CLKB are not referred to in the disclosure.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

1. The disclosure is objected to because of the following informalities: page 7 line 8 describes engine 110 being configured by a 66 bit signal composed of a 32 bit vector and 33 bit seed. The sum of 32 and 33 is not 66. Appropriate correction is required.

2. The disclosure is objected to because of the following informalities: page 9 line 24 recites, "(bits B_{26} to B_0)", but the examiner believes that it should read, "(bits B_{30} to B_0)". Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: page 9 line 34 recites, "LBST_STEP_STEPE", but the examiner cannot find this reference in FIG.9. Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: page 10 line 8 recites, "components 150", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

5. The disclosure is objected to because of the following informalities: page 13 lines 28 and 30 recite, "ASIC 100", but the examiner cannot find this reference in the drawings, and believes it should read "ASIC 150". Appropriate correction is required.

6. The disclosure is objected to because of the following informalities: page 13 line 31 recites, "925 including", but the examiner cannot find this reference in the drawings. Appropriate correction is required.

Claim Objections

7. Claims 1 and 17 are objected to because of the following informalities: the term "capable of" is not a positive limitation, and the examiner suggests that the term be removed. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 7 and 28 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The claims specify using a "paranoid check" for a purpose within a MBIST signature register. The same term is mentioned in the disclosure but the term was never defined. The examiner, being one with ordinary skill in the art, is unsure of what the applicant means when using this term.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites the limitation "the logic built-in self-test signature" in line 1. There is insufficient antecedent basis for this limitation in the claim.

10. Claims 7 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning,

the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term "paranoid check" in claims 7 and 28 is used by the claim to mean a test which the examiner is not familiar, while the accepted meaning is "to check again by another means." The term is indefinite because the specification does not clearly redefine the term.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1, 13, 16, 22, 26, 28, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Au et al., U.S. Patent No. 6681359.

As per Claim 1:

Au et al. teaches a built-in self-test controller (FIG.2 72), comprising; a built-in self-test engine (FIG.3 MBIST CONTROLLER 116) capable of executing a built-in self-test and generating an indication of whether the executed built-in self-test is

completed, and a built-in self-test signature including the indication (column 9 lines 25-33).

As per Claim 13:

Au et al. teaches a built-in self-test controller (FIG.2 72), comprising: means for executing a built-in self-test (column 1 lines 8-16, FIG.3 MBIST CONTROL 116) and generating an indication of whether the executed built-in self-test is completed; and means for storing the results of the executed built-in self-test, including the indication (column 9 lines 25-33).

As per Claim 16:

Dependent on Claim 13, Au et al. further teaches the built-in self-test controller of claim 13, wherein the executing means is a memory built-in self-test engine (column 1 lines 8-16, FIG.3 MBIST CONTROL 116) and the storing means is a memory built-in self-test signature register (FIG.3 114).

As per Claim 22:

Au et al. teaches a method for performing a built-in self-test (see Abstract), the method comprising: performing a built-in self-test (column 11 lines 61-61), including generating a indication of whether the built-in self-test is completed; and storing the indication (column 9 lines 25-34).

As per Claim 26:

Au et al. teaches the method of claim 22, wherein performing the built-in self-test includes performing a memory built-in self-test (column 2 lines 30-33) and storing the

indication includes setting a bit in a memory built-in self-test signature register (column 9 lines 25-34).

As per Claim 28:

The claim limits Claim 26 in that the signature includes paranoid check results. Since the examiner is unsure of the meaning of "paranoid check", it is assumed that the signature register of Claim 26 includes results of this kind (see column 9 lines 25-33 of Au et al.).

As per Claim 29:

Au et al. teaches a method for testing an integrated circuit device (see Abstract), the method comprising: interfacing the integrated circuit device with a tester (column 8 lines 29-31); performing a built-in self-test (column 8 lines 56-58), including generating a indication of whether the built-in self-test is completed (column 9 lines 25-34); storing the indication (column 9 lines 25-34); and reading the indication (column 10 lines 21-26).

As per Claim 32:

Au et al. teaches the method of claim 29, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols (column 10 lines 21-25).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. Claims 2, 6, 7, 8, 17, 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Au et al., U.S. Patent No. 6681359.

As per Claim 2:

Dependent on Claim 1, the controller is limited to a logic BIST engine (Motika et al. FIG.2 LBIST 34), and the self-test signature is a LBIST signature (Motika et al. column 3 lines 64-67 and column 4 lines 1-5). And, in view of the motivation in Claim 1 above, the claim is rejected.

As per Claims 6 and 8:

Motika et al. teaches a built-in self-test controller (FIG.2 50), comprising: a built-in self-test engine (FIG.2 ABIST 32) capable of executing a built-in self-test, and a built-in self-test signature (column 3 lines 53-63). However, Motika et al. fails to teach generating an indication of whether the executed built-in self-test is completed, and

including the indication in the signature. In an analogous art, Au et al., in testing memory arrays in a self-test device, takes the error data (if any) from an array (column 9 lines 7-24) that would be the signature data (FIG.3 114), and appends a TEST_DONE bit along with the signature (column 9 lines 25-33). And Au et al., in column 2 lines 18-27 in reciting the attributes of the invention, boasts of a better means to retrieve information within an MBIST while not requiring a large number of device pins. One with ordinary skill in the art at the time of the invention, motivated by Au et al., would combine the two references, thus the claims are rejected.

As per Claim 7:

The claim limits Claim 6 in that the signature includes paranoid check results. Since the examiner is unsure of the meaning of "paranoid check", it is assumed that the signature register of Claim 6 includes results of this kind (see column 9 lines 25-33 of Au et al.). And in view of the motivation previously stated, the claim is rejected.

As per Claim 17:

As an independent claim, the claim specifies an integrated circuit device (Motika et al. column 1 lines 5-8), comprising: a plurality of memory components (Motika et al., FIG.2 36); a logic core (Motika et al. FIG.2 38); a testing interface (Motika et al. FIG.2 60); and a built-in self-test controller (Motika et al. FIG.2 60), including: a built-in self-test engine capable of executing a built-in self-test on one of the memory components (Au et al. FIG.3 116 and 136) and the logic core and storing the results thereof (Au et al. FIG.3 114), wherein the results include an indication of whether an executed built-in self-test is completed; and a register capable of storing the results of

an executed built-in self-test, including the indication (Au et al. column 9 lines 25-34). And in view of the motivation for Au et al. above, the claim is rejected.

As per Claim 19:

Dependent on Claim 17, Au et al. further teaches a built-in self-test controller (FIG.3 112), comprising: a MBIST engine (FIG.3 116), and a MBIST signature register (FIG.3 114 and column 9 lines 25-33). And in view of the previous motivation for Au et al., the claim is rejected.

As per Claim 21:

Dependent on Claim 17, the claim limits the test interface to being a JTAG tap controller. Au et al., in the Abstract teaches such an interface, and in view of the motivation for Au et al. elsewhere, the claim is rejected.

13. Claims 3, 5 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Au et al., U.S. Patent No. 6681359 as applied to Claim 2 above, and further in view of Koproski et al., U.S. Patent No. 6671838.

As per Claim 3:

The claim is dependent on Claim 2, and limits the LBIST to comprise an LBIST state machine and pattern generator. In an analogous art, Koproski et al., in column 3 lines 1-5 teaches a state machine for this LBIST device, and, in FIG.1, Koproski et al. teaches a pattern generator 4. And in column 1 lines 1-67 and column 2 lines 1-28, the reference states the advantage of using a special analysis system for creating weighted patterns for testing in an LBIST. One with ordinary skill in the art at

the time of the invention, motivated by Koproski et al., would combine the references, and so the claim is rejected.

As per Claim 5:

The examiner has previously rejected this claim because the LBIST lacks antecedent basis. However, the examiner has interpreted the claim as referencing a BIST instead of an LBIST for the purpose of this rejection. Based on Claim 1, the limitation is that the BIST signature comprises a MISR. Koproski et al., in FIG.1 12 specifies such a register in the teachings. And in view of the motivation of Koproski et al. in an earlier rejection herein, the claim is rejected.

As per Claim 18:

Dependent on Claim 17, the limitation is that the BIST signature comprises a MISR. Koproski et al., in FIG.1 12 specifies such a register in the teachings, and Au et al. adds a "done" and "error" indicator (column 8 lines 56-67 and column 9 lines 1-5) to the signature (column 9 lines 25-34). And in view of the motivation of Koproski et al. in an earlier rejection herein, the claim is rejected.

14. Claims 4 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Au et al., U.S. Patent No. 6681359, and in view of Koproski et al., U.S. Patent No. 6671838 as applied to Claims 3 and 23, and further in view of Zuraski et al., U.S. Patent No. 6560740, Lo et al., U.S. Patent No. 5661732, and Wong et al., U.S. Patent No. 6636997. The LBIST state machine in Claims 3 and 23 is further limited to a reset state entered via an external signal. Zuraski et al. enters a state via an external reset signal (Zuraski et al, column 10 lines 31-36),

but does not begin initializing the device with an LBIST run signal. In an analogous art, Lo et al., enters a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), and suggests a similar LBIST on the same chip (column 6 lines 9-12). And finally, Wong et al. in column 6 lines 26-50 teaches the states of scan, step, and complete (done) as specified by the applicant's claim. Wong et al., in column 2 lines 62-67, describes an advantage of the invention as being capable of both pseudo-random and functional testing. And in view of the motivations elsewhere for Zuraski et al. and Lo et al., and in view of Wong et al., one with ordinary skill in the art at the time of the invention, would combine all of the references above, thus the claims are rejected.

15. Claims 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Au et al., U.S. Patent No. 6681359 as applied to Claim 6 above, and further in view of Zuraski Jr. et al., U.S. Patent No. 6560740. Dependent on Claim 6, Claim 9 limits the MBIST engine to comprise a MBIST state machine while Claim 11 limits a plurality of same, and a nested MBIST engine driving the state machine. In an analogous art, Zuraski Jr. et al. teaches the same hierarchy where an MBIST state machines (FIG.1 20a, 20b) are driven by an MBIST engine (FIG.1 18) as is described in column 5 lines 40-54. And Zuraski Jr. et al., professes the advantages (column 2 lines 10-18) of a readily programmable BIST that would not need constant revision as needs change. One with ordinary skill in the art at the time of the invention, motivated as suggested by Zuraski Jr. et al., would combine the references, and so the claims are rejected.

16. Claims 10, 12 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, in view of Au et al., U.S. Patent No. 6681359 as applied to Claim 26, and in view of Zuraski Jr. et al., U.S. Patent No. 6560740 as applied to Claims 9 and 11 above, and further in view of Lo et al., U.S. Patent No. 5661732. The claims, dependent on Claim 9, 11 and 26 above, further limit the controller/method wherein the state machine comprises a reset state entered upon an external reset signal (Zuraski et al, column 10 lines 31-36). However Zuraski et al. does not further limit the machine to flushing and testing. In an analogous art, Lo et al., upon entering a 1st state subsequent to a start ABIST signal (Lo et al. column 5 lines 6-8), the next state produces internal resets of registers, and then as a programmable option, a flush of the memory may occur (column 13 lines 6-10) and then subsequent testing (same reference) may take place. At the end of the test, a state described by column 5 lines 17-35 occurs with the initiation of a test done signal (FIG.1 26). In Lo et al. column 2 lines 38-40 lists an advantage of the invention as being an improvement in test time and test coverage. One with ordinary skill in the art at the time of the invention, motivated by Lo et al., would combine the references, and so the claims are rejected.

17. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, in view of Motika et al., U.S. Patent No. 5982189. Dependent on Claim 13, the controller is limited to a logic BIST engine (Motika et al. FIG.2 LBIST 34), and the self-test storing means is a LBIST signature register (Motika et al. column 3 lines 64-67 and column 4 lines 1-5). Motika et al., recites an advantage of the invention as a better way to stress the chip under test without utilizing excess space on the chip

(column 1 lines 65-67 and column 2 lines 1-4). And, one with ordinary skill in the art at the time of the invention, motivated by Motika et al., would combine the two art, and thus the claim is rejected.

18. Claims 15, 23, 25, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Au et al., U.S. Patent No. 6681359, as applied to Claims 13, 22 and 29 above, and in view of Koproski et al., U.S. Patent No. 671838. Dependent on Claim 13 or 22 or 29, the limitation is that the BIST signature comprises a MISR. Koproski et al., in FIG.1 12 specifies such a register in the teachings, and Au et al. adds a "done" and "error" indicator (column 8 lines 56-67 and column 9 lines 1-5) to the signature (column 9 lines 25-34). And in view of the motivation of Koproski et al. in an earlier rejection herein, the claims are rejected.

19. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al., U.S. Patent No. 5982189, and in view of Au et al., U.S. Patent No. 6681359 as applied to Claim 17 above, and further in view of Kim et al., U.S. Patent No. 6148426. Dependent on Claim 17, this claim limits a memory device to being a static random access memory. In an analogous art, Kim et al. teaches an MBIST (see Abstract) that is used for testing an sram (see Title). Citing a savings in BIST size and cost (column 2 lines 55-61), Kim et al. would motivate one with ordinary skill in the art at the time of the invention to combine the art for the purpose of testing sram memories.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
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